REMARKS/ARGUMENTS

The Office Action has been carefully considered. The issues raised are traversed and addressed below with reference to the relevant headings and paragraph numbers appearing under the Detailed Action of the Office Action.

Specification

The specification has been amended at Page 1. The first paragraph has been deleted and replaced with a paragraph entitled "Cross-Reference to Related Applications", showing the correct references. A replacement Declaration is enclosed. The Applicant submits that this amendment introduces no new matter.

Claim Rejections – 35 USC § 112

The Examiner has rejected claim 1 on the basis that it is not based on an enabling disclosure contained in the description. In particular, the Examiner notes that there is no enabling disclosure concerning the features of "drive circuitry", "a plurality of inlet channels" and "nozzle arrangements", a "passive nozzle chamber structure", a "dynamic nozzle chamber structure", and an "elongate micro-electromechanical actuator" which are disclosed in claim 1. The Applicant respectfully disagrees with this rejection and requests the Examiner's reconsideration of the rejection in view of the following comments set out below.

The Applicant notes that an enabling disclosure is provided for the "drive circuitry" at page 12, lines 6-15 of the description. That is:-

> *"A CMOS drive circuitry layer 20 is formed on the wafer 12. The CMOS layer 20 can, in accordance with standard techniques, include multi-level metal layers sandwiched between oxide layers and preferably at least a two level metal process is utilized. In order to reduce the number of necessary processing steps, the masks utilized include areas that provide for a build up of an aluminum barrier 21 which can be constructed from a first level 22 of aluminum and second level 23 of aluminum. Additionally, aluminum portions 24 are provided which define electrical contacts to a subsequent heater layer. The aluminum barrier 21 is important for providing an effective barrier to the possible subsequent etching of the oxide within the CMOS layer 20 when a sacrificial etchant is utilized in the construction of the nozzle arrangement 10 with the etchable material preferably being glass layers."*

It is further noted that an enabling disclosure is provided in respect of the "plurality of ink inlet channels" at page 12 lines 27-29 of the description in which it is referred to as "ink supply channels" (13). This feature is also clearly depicted in Figs. 1-3 by the reference numeral (13).

An enabling disclosure is also provided in respect of the "nozzle arrangements" at page 12, lines 31-34 of the description – that is:

> *"Many ink jet nozzle arrangements are formed at a time, on a selected wafer base 12 utilizing standard semi-conductor processing techniques in addition to micro-machining and micro-fabrication process technology further details of this form of fabrication are set out in further detail further on in this specification."*

Figures 6-15 provides an enabling disclosure for the formation of the inkjet "nozzle arrangements". A detailed description as to the formation of the nozzle arrangements with reference to Figs 6-15 is provided between page 13 line 26 and page 15 line 18 – that is:

> *"The various steps involved in the construction of an array of ink jet nozzle arrangements are explained in Figs. 6 to 15.*
>
> *1. Turning initially to Fig. 6, the starting position comprises a silicon wafer 12 including a CMOS layer 20 which has nitride passivation layer 26 and which is surface finished with a chemical - mechanical planarization process.*
>
> *2. The nitride layer is masked and etched as illustrated in Fig. 7 so as to define portions of the nozzle arrangement and areas for interconnection between any subsequent heater layer and a lower CMOS layer.*
>
> *3. Next, a sacrificial oxide layer is deposited, masked and etched as indicated in Fig. 8 with the oxide layer being etched in those areas where a subsequent heater layer electronically contacts the lower layers.*
>
> *4. As illustrated in Fig. 9, a 1 micron layer of PTFE is deposited and first masked and etched for the heater contacts to the lower CMOS layer and then masked and etched for the heater shape.*
>
> *5. Next, as illustrated in Fig. 10, the gold heater layer 30, 31 is deposited. Due to the fact that it is difficult to etch gold, the layer can be conformally deposited and subsequently portions removed utilizing chemical mechanical planarization so as to leave those portions associated with the heater element. The processing steps 4 and 5 basically comprise a dual damascene process.*
>
> *6. Next, a top PTFE layer is deposited and masked and etched down to the sacrificial layer as illustrated in Fig. 11 so as to define the heater shape. Subsequently, the surface of the PTFE layer is plasma processed so as to make it hydrophilic. Suitable processing can exclude plasma damage in an ammonia atmosphere. Alternatively, the surface could be coated with a hydrophilic material.*
>
> *7. A further sacrificial layer is then deposited and etched as illustrated in Fig. 12 so as to form the structure for the nozzle chamber. The sacrificial layer is then masked and etched in order to define a deposition area for the nozzle chamber walls.*
> *8. As illustrated in Fig. 13, the nozzle chamber is formed by conformally depositing three microns of nitride and etching a mask nozzle rim to a depth of one micron for the nozzle rim (the etched depth not being overly time critical). Subsequently, a mask is utilized to etch the ink ejection port 35 in addition to the sacrificial layer etchant holes 36.*

9. As illustrated in Fig. 14, the backside of the wafer is masked for the ink channels and plasma etched through the wafer. A suitable plasma etching process can include a deep anisotropic trench etching system such as that available from SDS Systems Limited (See) "Advanced Silicon Etching Using High Density Plasmas" by J.K. Bhardwaj, H. Ashraf, page 224 of Volume 2639 of the SPIE Proceedings in Micro Machining and Micro Fabrication Process Technology).

10. As illustrated in Fig. 15, the sacrificial layers are etched away utilizing a sacrificial etchant such as hydrochloric acid. Subsequently, the portion underneath the actuator that is around the ink channel is plasma processed through the backside of the wafer to make the panel end hydrophilic."

The feature of the "passive nozzle chamber structure" is referred to as the "nozzle chamber" within the description and an enabling disclosure as to the formation of this feature is provided between page 14 line 33 to page 15 line 6 as follows:

"8. As illustrated in Fig. 13, the nozzle chamber is formed by conformally depositing three microns of nitride and etching a mask nozzle rim to a depth of one micron for the nozzle rim (the etched depth not being overly time critical). Subsequently, a mask is utilized to etch the ink ejection port 35 in addition to the sacrificial layer etchant holes 36."

The feature of the "dynamic nozzle chamber structure" is referred to within the description as the "ink ejection port" (35). An enabling disclosure of this feature is thus provided at page 13 lines 18-24 as follows:

"On top of the actuator 14 are formed nitride side wall portions 33 and a top wall portion 34. The wall portions 33 and the top portions 34 can be formed via a dual damascene process utilizing a sacrificial layer. The top wall portion 34 is etched to define the ink ejection port 35 in addition to a series of etchant holes 36 which are of a relatively small diameter and allow for effective etching of lower sacrificial layers when utilizing a sacrificial etchant. The etchant holes 36 are made small enough such that surface tension effects restrict the possibilities of ink being ejected from the chamber 32 via the etchant holes 36 rather than the ejection port 35."

The feature of an "electro-mechanical actuator" is referred to as the "thermal actuator" (14) in the description, and, an enabling description is provided between page 10 line 31 and page 11 line 25 of the description.

In view of the clear support provided within the description for the features of claims 1 raised by the Examiner, the Applicant requests that the claims rejection made under section 112 be properly withdrawn.

Double Patenting

In paragraphs 8-15 of the Office Action, the Examiner has rejected claims 1 to 6 on the grounds of a non-statutory type double-patenting rejection. In view of this, we are filing herewith a terminal disclaimer to overcome the double patenting objection.

In light of the above, it is respectfully submitted that the claim rejections have been successfully traversed and addressed. Accordingly, it is respectfully submitted that the claims 1-6, and the application as a whole with these claims, are allowable, and a favourable reconsideration is therefore earnestly solicited.

Very respectfully,

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